SEASONAL SCHOOL PROPOSAL

SEASONAL SCHOOL ON "NEUROMORPHIC COMPUTING and IN MEMORY COMPUTING USING NON-VOLATILE MEMORY DEVICES (HYBRID)

Speaker Profile Details:

Dr Kim Tae Hyoung

Prof. Tony T. Kim received the B.S. and M.S. degrees in electrical engineering from Korea University, Seoul, Korea, in 1999 and 2001, respectively. He received the Ph.D. degree in electrical and computer engineering from the University of Minnesota, Minneapolis, MN, USA in 2009. From 2001 to 2005, he worked for Samsung Electronics where he performed research on the design of high-speed SRAM memories, clock generators, and IO interface circuits. In 2007 ~ 2009 summer, he was with IBM T. J. Watson Research Center and Broadcom Corporation where he performed research on isolated NBTI/PBTI measurement circuits and SRAM Mismatch measurement test structure, and battery backed memory design, respectively. In November 2009, he joined Nanyang Technological University where he is currently an associate professor. His current research interests include low power and high performance digital, mixed-mode, and memory circuit design, ultra-low voltage sub- threshold circuit design for energy efficiency, variation and aging tolerant circuits and systems, approximate computing, and circuit techniques for 3D ICs.

He received Best Demo Award at 2016 IEEE APCCAS, International Low Power Design Contest award at 2016 IEEE/ACM ISLPED, a best paper award at 2014 and 2011 ISOCC, 2008 AMD/CICC Student Scholarship Award, 2008 Departmental Research Fellowship from U. of Minnesota, 2008 IEEE DAC/ISSCC Student Design Contest Award, 2008 Samsung Humantec Thesis Award (Bronze Prize), 2005 ETRI Journal Paper of the Year Award, 2001 Samsung Humantec Thesis Award (Honor Prize), and 1999 Samsung Humantec Thesis Award (Silver Prize). He is an author/co-author of around 120 journal and conference papers and holds 17 US and Korean patents. He serves as an Associate Editor of IEEE Transactions on Very Large Scale Integration (VLSI) Systems, IEEE Access, and IEIE Journal of Semiconductor Technology and Science (JSTS). He has also served as a technical committee member of various conferences such as IEEE Asian Solid-State Circuits Conference (A-SSCC), IEEE International Symposium on Circuits and Systems (ISCAS), IEEE/ACM International Symposium on Low Power Electronics and Design (ISLPED), etc. He was the Chair of IEEE SSCS Singapore Chapter in 2015~2016. He is a senior member of IEEE.

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Dr FONG, Xuanyao Kelvin

Xuanyao Fong received the Ph.D. and B.Sc. degrees in electrical engineering from Purdue University, West Lafayette, IN, in 2014 and 2006, respectively.

From January to August 2007, he was an Intern Engineer with Advanced Micro Devices, Inc., Boston Design Center, Boxboro, MA. He was a Research Assistant and then Postdoctoral Research Assistant to Professor Kaushik Roy in the Nanoelectronics Research Laboratory, Purdue University, from August 2007 to May 2015. He was then a Research Scientist in the Institute of Microelectronics, Agency for Science, Technology and Research (A*STAR) from June 2015 to November 2016. Currently, he is an Assistant Professor in the Department of Electrical & Computer Engineering at the National University of Singapore. His research interests include devices-to-systems co-design methodologies for Si and non-Si nanoelectronics; design of high performance and ultralow power logic and memory systems using spintronic devices, circuits, and architectures; and non-Boolean and analog computing paradigms using emerging technologies.

Dr. Fong received the AMD Design Excellence Award at Purdue in 2008, and the best paper award at the 2006 International Symposium on low power electronics and design.

Dr Thomas Kämpfe

Thomas Kämpfe (Member, IEEE) received the Diploma and PhD degrees in physics from TU Dresden, in 2011 and 2016, respectively. He was a senior scientist with Fraunhofer IPMS, Center Nanoelectronic Technologies. After research visiting scholar positions with the University of Colorado, Boulder and Stanford University, he joined the Fraunhofer Society in 2017. He authored and coauthored more than 100 peer-reviewed journal papers and conference proceedings. His main research interests include CMOS compatible ferroelectrics for advanced emerging memories, analog in-memory computing paradigms/architectures, high-frequency electronics, pyro- & piezo-electronics as well as RF/mmWave devices & circuits in CMOS and SOI technologies.

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Damien Querlioz is a tenured CNRS Researcher at the Centre de Nanosciences et de Nanotechnologies of Université Paris-Saclay (formerly known as Université Paris-Sud) and CNRS. He was first trained at Ecole Normale Supérieure Paris as a physicist and at Ecole Supérieure d'Electricité as a microelectronics engineer. He received the Ph.D. degree from Université Paris-Sud in 2009. He was then a Postdoctoral Scholar at Stanford University and at the Commissariat a l'Energie Atomique.

Damien Querlioz develops new concepts in nanoelectronics relying on bio-inspiration. He believes that nanoelectronics can allow inventing highly energy-efficient forms of memory-centric computing. He investigates stochastic approaches, the use of spintronics devices for bioinspired systems, and the connection between bioinspired memories and Bayesian inference. His research interests have also included the physics of advanced nanodevices. He has developed the Wigner Monte Carlo approach to simulate and understand quantum transport in nanometer-scale devices.

In 2016, Damien Querlioz received the Habilitation degree (HDR). Since 2017, he is the coordinator of the interdisciplinary INTEGNANO research group, with amazing colleagues working around an integrative and multidisciplinary approach to the development of novel charge and spin based devices, as well as fantastic students and postdocs.

Damien Querlioz is a member of the bureau of GDR Biocomp, a French network to facilitate interdisciplinary exchanges around the realization of bio-inspired hardware systems, and has been a management committee member of the MEMOCIS COST action, a European-wide scientific and technology knowledge platform on memristive technology. He has coauthored 9 book chapters, more than 150 journal articles and conference proceedings and given more than 75 invited talks at national and international workshops and conferences. He has also coauthored the book "The Wigner Monte-Carlo Method for Nanoelectronic Devices" (London: ISTE; Hoboken: Wiley, 2010) with Philippe Dollfus. In 2017, he received a CNRS Bronze medal. He has also been a co-recipient of the 2017 IEEE Guillemin-Cauer Best Paper Award and of the 2018 IEEE Biomedical Circuits and Systems Best Paper Award.

The research of Damien Querlioz has been funded by the Seventh Framework Programme of the European Union (FETOPEN BAMBI), Agence Nationale de la Recherche, Région Ile-de-France/DIM NANO-K and Ministère de l'écologie, du développement durable et de l'énergie. In recent years, he also received funding from CNRS/Mission pour l'Interdisciplinarité and CNRS/INSIS. Starting March 2017, he has been leading the NANOINFER project, funded by a European Research Council Starting Grant for a duration of 5 years.

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Dr. Catherine Schuman

Catherine (Katie) Schuman is an Assistant Professor in the Department of Electrical Engineering and Computer Science at the University of Tennessee (UT). She received her Ph.D. in Computer Science from UT in 2015, where she completed her dissertation on the use of evolutionary algorithms to train spiking neural networks for neuromorphic systems. Katie previously served as a research scientist at Oak Ridge National Laboratory, where her research focused on algorithms and applications of neuromorphic systems. Katie co-leads the TENNLab Neuromorphic Computing Research Group at UT. She has over 70 publications as well as seven patents in the field of neuromorphic computing. She received the Department of Energy Early Career Award in 2019. Katie is a senior member of the Association of Computing Machinery and the IEEE.

Dr. Merlyne De Souza

I graduated with a BSc in Physics and Mathematics (1985) from the University of Mumbai, a BE. in Electronics and Communications Engineering (1988) from the Indian Institute of Science, Bangalore and a PhD from the University of Cambridge (1994).I joined as a Junior Research fellow in ‘95, was promoted to a Senior Research fellow in ‘98 and was appointed Professor in Electronics and Materials at the Emerging Technologies Research Centre, De Montfort University in 2003.I joined the EEE department at Sheffield as Professor of Microelectronics in 2007. I work in multi-disciplinary research focused on the physics of devices, materials and their microelectronic applications in computing, communications and energy conversion.Until now, microelectronics has relied on the versatility of silicon CMOS to deliver enhancement in performance by scaling the MOS transistor. I have worked on

various aspects of CMOS such as reliability, high-k gate oxides and Indium for retrograde channels, first introduced in production at the 65 nm node.However, scaling (as we know it) is now nearing an end and alternate materials and device architectures are required for future semiconductor applications.

Supervised learning for image and speech recognition, autonomous driving and medical diagnosis in Artificial Intelligence (AI) presently rely on CMOS based deep neural networks.These are inherently power-hungry due to a continuous exchange of information between the required large volume of memory and processing units.

It is expected that such Von Neumann architectures will be replaced by neuromorphic systems that are more akin to a biological brain.

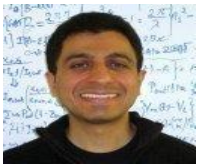
Our team has recently demonstrated ZnO/Ta2O5 solid electrolyte thin film transistors with synaptic capabilities.I am interested in exploring such memristive devices in neuromorphic applications, electrochemical storage and flexible electronics for health.My interest in more efficient semiconductors, smart materials and systems that leave a smaller footprint on the environment, spans to GaN for power and RF applications, that I have previously explored in equivalent silicon- based device technologies such as the IGBT and the RF LDMOSFET.These are driven by the automotive, aerospace, space, renewables, telecoms and consumer/industrial electronics sectors.Our recent work includes a new class of harmonic RF power amplifiers with record efficiency and output power prototyped using commercial GaN devices.We are also working towards a p-type MOSHFET and magnetic thin films for “CMOS in GaN” in power management integrated circuits and current sensors.

Dr. Shubham Sahay

Shubham Sahay (Senior Member, IEEE) received the B.Tech. degree (Hons.) in electronics engineering with four gold medals and several cash prizes from the Indian Institute of Technology (BHU) Varanasi in 2014, and the Ph.D. degree in electrical engineering from Indian Institute of Technology (IIT) Delhi in 2018. He is an Assistant Professor with the Department of Electrical Engineering, IIT Kanpur, India. Prior to joining IIT Kanpur, he worked as a Postdoctoral Research Scholar with the University of California at Santa Barbara, Santa Barbara, from 2018 to 2020. He has authored a book on “Junctionless Field Effect Transistors: Design, Modeling and Simulation” which is published by the (Wiley- IEEE Press). He has also published several peer-reviewed articles on topics, including semiconductor device design and modeling, neuromorphic computing, and hardware security primitives utilizing emerging non-volatile memories. His current research interests include hardware neuromorphic computing platforms, hardware security primitives, novel device architectures for sub-10 nm regime, analytical and compact modeling of semiconductor devices and non-volatile memories, and spintronics. He is the recipient of the IEEE EDS

Early Career Award in 2023 and the Young Associate 2023 of Indian National Academy of Engineering. He is an Editor of IETE Technical Review and a Review Editor for Frontiers in Neuroscience: Neuromorphic Engineering and Frontiers in Electronics: Integrated Circuits and VLSI. He is the Chair of IEEE EDS UP Section. He also appeared in the list of Golden Reviewers for IEEE Transactions on Electron Devices and IEEE Electron Device Letters from 2016 to 2020.

Dr. Bhavin Shastri



Bhavin J. Shastri is an Assistant Professor of Engineering Physics at Queen's University, Canada, and a Faculty Affiliate at the Vector Institute for Artificial Intelligence, Canada. He was an Associate Research Scholar (2016-2018) and Banting/NSERC Postdoctoral Fellow (2012-2016) at Princeton University. He received a Ph.D. degree in electrical engineering (photonics) from McGill University in 2012. With research interests in silicon photonics, neuromorphic photonic computing, and quantum machine learning, he has published more than 100 journal articles and 115 conference proceedings, seven book chapters, and given over 100 invited talks and lectures, including eight keynotes. He is a co-author of the book Neuromorphic Photonics (Taylor & Francis, 2017), a term he helped coin.

Dr. Shastri is the recipient of the 2022 iCANX Young Scientist Award, the 2022 SPIE Early Career Achievement Award, and the 2020 IUPAP Young Scientist Prize in Optics "for his pioneering contributions to neuromorphic photonics" from ICO. He is a Senior Member of Optica and IEEE, recipient of the 2014 Banting Postdoctoral Fellowship from the Government of Canada, the 2012 D. W. Ambridge Prize for the top graduating Ph.D. student at McGill, and an IEEE Photonics Society 2011 Graduate Student Fellowship, amongst others awards.

Dr. Shady Agwa

Shady Agwa (IEEE Member) is a Research Fellow at the Centre for Electronics Frontiers CEF, The University of Edinburgh (UK). He received his BSc and MSc degree from Assiut University (Egypt), both in Electrical Engineering. He got his PhD in Electronics Engineering from The American University in Cairo (Egypt) in 2018. Following his PhD, he joined the Computer Systems Laboratory at Cornell University (USA) as a Postdoctoral Associate for two years. In 2021, Shady joined the Centre for Electronics Frontiers at the University of Southampton (UK) as a Senior Research Fellow and then as a Research Fellow at the University of Edinburgh (UK). His research interests span across VLSI and Computer

Architecture using conventional and emerging technologies for AI applications. His work focuses on unconventional ASIC-Driven AI Architectures which cover In-Memory Computing, Stochastic Computing, Systolic Arrays, Content-Addressable Memories, Beyond-Von Neumann Architectures and Energy-Efficient Digital ASIC Design.

Dr. Laura Bégon-Lours

Researcher in Materials for AI Hardware. Polyvalent, autonomous, in quest of conceptual and technological challenges. After receiving a Marie-Curie Individual Fellowship, I led the research on ferroelectric synapses for analog AI hardware at IBM Research Zurich. ESPCI- PSL engineer, I navigate at the interface between academia and industry. Since my PhD project at CNRS-Thales (2012) and up to today, my research explores ferroelectric field- effects in oxides. Skills: Correlated Oxides, Thin-Films, Growth, Materials Characterisation, Clean Room, Lithography, Cryogenics, Electrical Measurements.