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A Report on
SERB sponsored 3-Day National Seminar on
"Recent Trends and Challenges in VLSI Circuits, Devices and Architectures"
Organized by Department of Electronics and Communication Engineering
from 23.01.2024-25.01.2024

Submitted by: Dr. Nehru Kandasamy, Professor, Department of Electronics and Communication Engineering

Event Coordinators:

1. **Dr. Nehru Kandasamy, Professor, Department of Electronics and Communication Engineering.**
2. **Dr. Grande Nage Jyothi, Assistant Professor, Department of Electronics and Communication Engineering.**
3. **Dr. R. Kiran Kumar, Assistant Professor, Department of Electronics and Communication Engineering.**
4. **Dr. Vivek Jain, Assistant Professor, Department of Electronics and Communication Engineering.**

Resource Persons:

1.	Dr Noor Mahammad Sk Associate Professor	VLSI Architectures for Signal Processing	Computer Science and Engineering, Indian Institute of Information Technology, Design and Manufacturing (IIITDM) Kancheepuram
2.	Dr. Sakthivel R	VLSI Architectures for AES Encryption	Dr. R. Sakthivel, Professor, Department of Micro and Nano Electronics, Vellore Institute of Technology
3.	Dr. D. Vishnu Vardhan Professor	Optimization of Placement and Routing in ASIC design	Electronics and Communication Engineering, Jawaharlal Nehru Technological University Anantapur
4.	Dr Sridevi Sriadibhatia Professor	Low Power VLSI Design	School of Electronics Engineering, Micro & Nanoelectronics Department, Vellore Institute of Technology
5.	Dr. Nehru Kandasamy Professor	Introduction to Non-volatile Memory Devices	Department of ECE Madanapalle Institute of Technology and Science
6.	Dr. Jayanarayan T Tude Assistant Professor	Digital VLSI Test and Verification and Post-Silicon Debug	Computer Science and Engineering Indian Institute of Technology Tirupati
7.	Dr. Sreelal Sreedharan Pillai Sci/Engineer-G, Division Head	VLSI Design and Intelligent Systems	Vikram Sarabhai Space Centre (VSSC) Indian Space Research Organization Trivandrum-695022, Kerala, INDIA
8.	Dr. V. Ramesh Kumar	Modern VLSI Circuit Design Using Graphene	Department of ECE, IIIT Sricity
9.	Dr. Swapnil Bhuktare Assistant Professor	Modelling & Simulation of Nano Transistor, their fabrication and Characterization	Electrical Engineering Indian Institute of Technology Tirupati
10.	Dr.D.Rukmani Devi Professor	FPGA Architectures for Machine Learning	Department of ECE, R.M.D Engineering College, Chennai

Event Description:

The SERB sponsored 3-Day National Seminar titled “Recent Trends and Challenges in VLSI Circuits, Systems and Architectures” was conducted from 23rd January 2024 to 25th January 2024. The national seminar aimed to enhance the faculty members, undergraduate students and research scholar’s skills and knowledge in the domain of semiconductors. The resource person for the national seminar was Dr Noor Mahammad S K, Dr. Sakthivel R, Dr. D. Vishnu Vardhan, Dr Sridevi Sriadibhatia, Dr. Nehru Kandasamy, Dr. Jayanarayan T Tude, Dr. Sreelal Sreedharan, Dr. V. Ramesh Kumar, Dr. Swapnil Bhuktare and Dr. D. Rukmani Devi. The event was inaugurated by Dr. P. Ramanathan, Vice principal (Academics) and encouraged the participants to learn VLSI design & Tools for research and chip design in the field of semiconductor. Dr. R. Thulasiram Naidu, Advisor R&D & Consultancy addressed about importance of VLSI in industry during his speech. Dr. Dr. S. Rajasekaran, Professor and Head of the the Department of Electronics and Communication Engineering appreciated the participation of national seminar and event coordinators.

Day-wise overview:

Day 1, 23rd January 2024: VLSI Architectures for Signal Processing, AES Encryption and Optimization of Placement and Routing in ASIC design

The program commenced with a ceremonial opening on Day 1, Where Dr. Nehru Kandasamy introduced the sponsors and welcomed Dr. Noor Mahammed SK and Dr. R. Sakthivel. The vice principal of MITS addressed the participants, emphasizing the significance of VLSI in engineering and technology. Dr. S. Rajasekaran, Head of the Electronics and Communication Engineering Department, provided insights into the seminar's importance. The keynote speakers from day 1 covered approximate computing for image processing applications, encryption techniques and physical design importance in ASIC. The session featured intriguing discussions with introspective questions and answer sessions among all the participants and the instructor.

Day 2, 24th January 2024: Low Power VLSI Design, Introduction to Non-Volatile Memory Devices and Low Power VLSI Testing for Edge SOC

The national seminar continued with low power VLSI design and techniques for power optimization and concept of non-volatile memory device are covered in the morning session and VLSI testing technique approached in the afternoon session. The highly interactive sessions allowed participants to grasp the theoretical and practical applications of these essential VLSI circuits and architectures. The keynote speaker from IIT and VIT covered practical applications of testing and test algorithm for system on chip.

Day 3, 25th January 2024: VLSI Design and Intelligent Systems, Modern VLSI circuit using graphene, Nano scale spintronic devices and FPGA Architecture for Machine Learning

In Day 3, focused on the rapidly evolving fields of machine learning using FPGA Architectures. The keynote speakers from ISRO, IIIT, IIT and R.M.D engineering college covered the topic related to Intelligent systems and recent fields in semiconductor. Dr Swapnil from IIT introduced the concept of nano devices and applications of nano device for neuromorphic computing. Dr. S.V. Ramesh Kumar has delivered the keynote talk related to VLSI circuit design using graphene for metal and circuit applications. The last session of the national seminar was handled by Dr. Rukmani Devi from R.M.D engineering college.