A Report on A Five-Day National Level Workshop on "Hands-On EDA Tools for Semiconductor Manufacturing"

Organized by Department of Electronics and Communication Engineering

Sponsored by MITS – IEEE, ComSoc (Hybrid Mode)

Date:20.01.2025 to 24.01.2025

Report Submitted by: Dr. G. Naga Jyothi, Dr. G. Naga Swetha and Mr. G Charan Kumar Assistant Professor Department of ECE.

Resource Person Details: Mr Navannetha krishanan Senior Application Engineer Entuple Technologies Bangalore; Dr. Narasimhulu Thoti, Scientific Researcher Microelectronics Research and University of Oulu 90570 Finland; Dr V Bharath Sreenivasulu Assistant Professor Department of Electronics and Manipal University.

Venue: Scaleup Room, MITS
Attendees: 15 M. Tech students and 45 Faculty members.
Mode of Conduct: Online and Offline
Report Received on 30.01.2024.

The Department of Electronics and Communication Engineering (ECE) successfully organized a **Five-Day National Level Workshop on Hands-On EDA Tools for Semiconductor Manufacturing** from **20th January 2025 to 24th January 2025** in the Scaleup Room. The workshop was sponsored by the **MITS IEEE Communication Society** and was aimed at providing participants with practical exposure to Electronic Design Automation (EDA) tools used in semiconductor manufacturing.

Workshop Objectives:

The primary objective of this workshop was to enhance participant's knowledge of cutting-edge EDA tools, covering aspects such as simulation, layout design, and process optimization for semiconductor device fabrication. This workshop provided attendees with a comprehensive understanding of the theoretical and practical dimensions of semiconductor manufacturing.

Workshop Brochure:

Inauguration Ceremony:

The workshop was inaugurated on **20th January 2025** in the presence of distinguished guests:

Dr. P. Ramanathan, Vice Principal (Academics) Dr. S. Rajasekaran, Professor & Head, Department of ECE

Dr. Ramanathan Vice Principal Academics his keynote speech, highlighted the significance of EDA tools in advancing semiconductor research and industry applications.

Dr. Rajasekaran HOD ECE delivered the welcome address, emphasizing the importance of hands-on learning in semiconductor technology.

The sessions were conducted by coordinators from the Department of ECE:

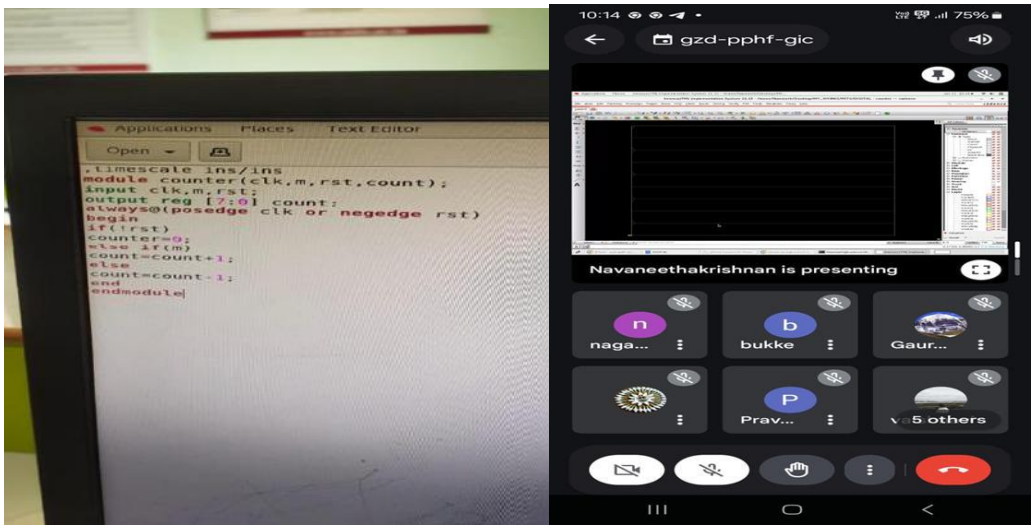
- Dr. G. Naga Jyothi, Assistant Professor Department of ECE
- Dr. G. Naga Swetha, Assistant Professor Department of ECE
- Mr. G. Charan Kumar, Assistant Professor Department of ECE

Day 1 – 20.01.2025

Morning Session – 11: 00 AM to 12:30PM

Resource Person: Mr. Navaneetha Krishanan Senior Application Engineer Entuple Technologies Bangalore.

Topic: Introduction to cadence tool using semi-custom design flow & Design of 8 bit counter from RTL to GDSII.



Mr. Navaneetha krishnan began with an introduction to semiconductor technology, its role in modern electronics, and the importance of EDA tools like Cadence and in the chip design process.

He emphasized the design flow in VLSI, starting from behavioural modelling to physical implementation.

Key challenges in semiconductor design, including power optimization, speed, and area minimization, were discussed.

Introduction to the Cadence Tool:

- A brief tutorial on Cadence Virtuoso, the industry's standard platform for IC design, was provided.
- Attendees were guided on how the tool integrates schematic design, simulation, and layout processes into a unified environment.
- The workshop aimed to provide hands-on experience with **Cadence EDA tools** for implementing a **counter** using a **semi-custom VLSI design flow**. The semi-custom methodology enables efficient digital design by leveraging pre-designed standard cells while allowing customization for performance optimization.

Objectives:

- Understanding the **semi-custom design flow** for ASIC development.
- Implementing a **counter circuit** using Cadence tools.
- Learning **functional verification, synthesis, placement & routing, and timing analysis**.

Tools Used:

The following **Cadence tools** were utilized:

- **Virtuoso** – Schematic & Layout Design
- **Xcelium** – Functional Simulation
- **Genus** – Logic Synthesis
- **Innovus** – Physical Design (Placement & Routing)

Design Flow Overview: The **semi-custom flow** for designing the counter included the following steps:
RTL Design:

- The **counter** was coded in **Verilog HDL**.
- It was designed as a **4-bit synchronous up-counter**.

Functional Verification:

- The Verilog design was simulated using **Xcelium** to verify its functionality.
- Testbenches were written to check count transitions and reset conditions.

Synthesis (Using Genus):

- The RTL was synthesized into a **gate-level netlist** using standard cell libraries.
- Synthesis reports (area, timing, power) were analyzed.

Placement & Routing (Using Innovus):

- The synthesized netlist was imported into **Innovus**.
- **Placement, Clock Tree Synthesis (CTS), and Routing** were performed.
- Design Rule Check (**DRC**) and Layout Versus Schematic (**LVS**) were run.

Timing & Power Analysis:

- **Static Timing Analysis (STA)** was conducted to check setup and hold time violations.
- **Power analysis** was done using **Voltus**.

Hands-on Experience:

During the workshop, the following tasks were performed:

- Writing and debugging **Verilog code** for the counter.
- Simulating the counter in **Xcelium** to verify its behavior.
- Running **synthesis in Genus** to generate the gate-level netlist.
- Performing **floorplanning, placement, and routing** using Innovus.
- Checking **DRC and LVS** for layout correctness.
- Running **timing and power analysis** for optimization.

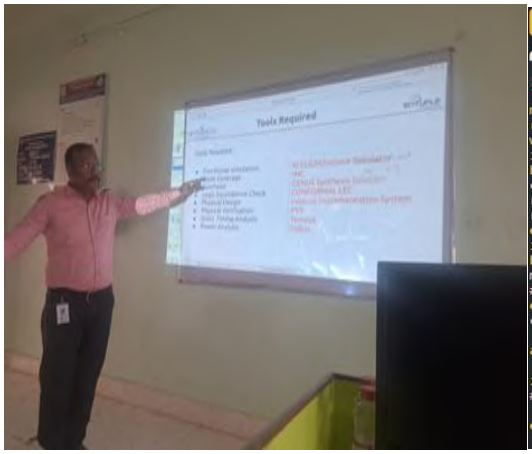
Results & Observations:

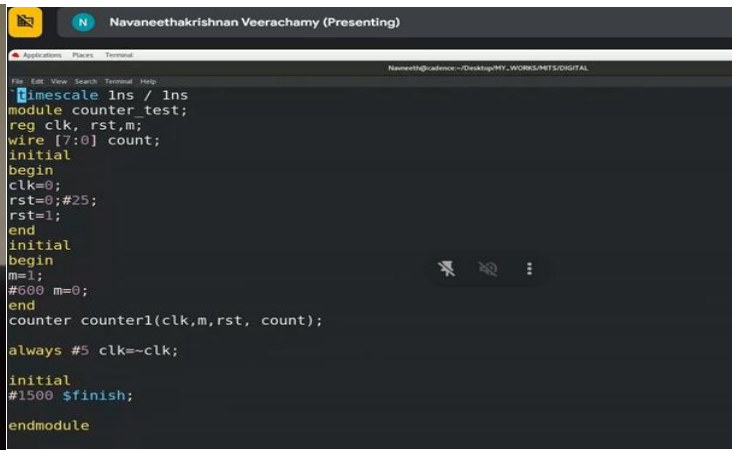
- The counter successfully **simulated** and matched the expected waveform.
- Post-synthesis **timing analysis** showed minor violations that were optimized.
- Physical design steps (floorplanning, placement, routing) were successfully completed.
- **DRC/LVS checks** were clean with no errors.
- Power consumption was analyzed, and optimizations were suggested

Practical Applications:

Mr. Navaneethakrishnan illustrated how these techniques are employed in designing modern ICs used in microprocessors, memory, and communication systems.

Case studies were presented to showcase the scalability of Cadence tools for industrial applications.





Day 1 – 20.01.2025

Afternoon Session – 02:00 PM to 05:00 PM

Topic: Physical Verification including DRC and LVS of Semiconductor design and Practical experience in designing, Simulating and Verifying semiconductor devices

Physical Verification: DRC and LVS:

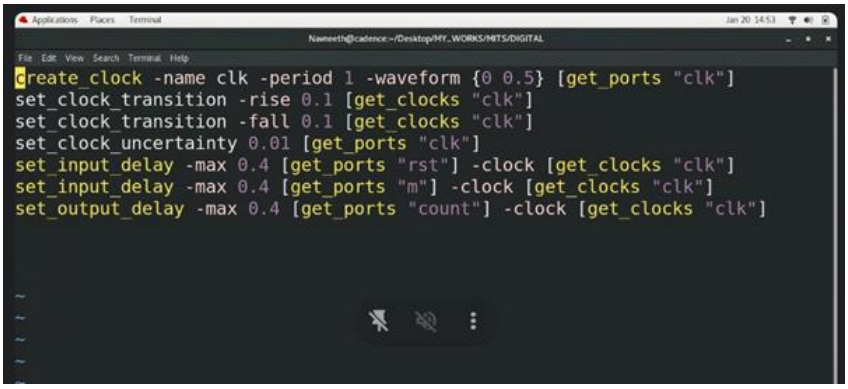
Physical verification is a critical phase in the semiconductor design lifecycle, ensuring that the fabricated chip will meet design intent and manufacturing constraints. Mr. Navaneethakrishnan's expertise lies in two essential components of physical verification:

Design Rule Check (DRC):

- **Overview:** DRC is performed to verify that the layout of a semiconductor design adheres to the manufacturing constraints set by the foundry.
- **Practical Experience:** Mr. Navaneethakrishnan has demonstrated excellence in leveraging industry-standard tools such as Cadence Assura, Synopsys IC Validator, and Mentor Graphics Calibre to perform DRC. He has resolved complex rule violations by optimizing layouts and aligning with technology node-specific constraints (e.g., 45nm, 90nm).

Layout Versus Schematic (LVS):

- **Overview:** LVS ensures that the physical layout corresponds accurately to the circuit schematic, verifying connectivity and identifying discrepancies.
- **Practical Experience:** He has extensive hands-on experience in running LVS to detect and rectify issues such as shorts, opens, and mismatched device parameters. His ability to debug and resolve these discrepancies ensures robust and error-free designs.



Practical Experience in Semiconductor Design and Simulation:

Mr. Navaneethakrishnan has substantial experience across the semiconductor design workflow, including:

Design:

- Skilled in designing CMOS circuits, including analog, digital, and mixed-signal layouts.
- Expertise in schematic capture using tools like Cadence Virtuoso and Mentor Graphics Design Architect.

Simulation:

- Proficient in performing pre- and post-layout simulations to analyse the performance of semiconductor devices.
- Experience with SPICE simulation tools for transient, DC, and AC analyses.

Verification:

- Competent in integrating Physical Verification tools into EDA workflows for seamless DRC and LVS checks.
- Practical involvement in tape-out processes, ensuring that the designs are error-free before fabrication.

Day 2 – 21.01.2025
Morning Session: 10: 00 AM to 01:00 PM
Resource Person: Mr. Navaneetha krishanan, Senior Application Engineer, Entuple Technologies, Bangalore.
Topic: Analog Circuit Design using cadence virtuoso

Key Topics Covered

Introduction to Analog Circuit Design:

- Basic concepts of analog circuits.
- Importance of analog design in modern electronic systems.
- Comparison between analog and digital design methodologies.

Overview of Cadence Virtuoso:

- Introduction to the Cadence Virtuoso platform.
- Features and capabilities of Virtuoso in analog circuit design.
- Interface navigation and basic tool setup.

Design Workflow:

- Schematic capture and circuit simulation.
- Device modeling and parameter extraction.
- Importance of SPICE models in analog design.

Simulation and Analysis:

- Performing transient, AC, and DC analysis.
- Noise and distortion analysis for analog circuits.
- Design optimization using simulation results.

- **Layout Design and Verification:**

- Principles of layout design in analog circuits.
- Parasitic extraction and its impact on circuit performance.
- Design rule checks (DRC) and layout versus schematic (LVS) verification.

Hands-On Demonstration:

The session included a hands-on demonstration of designing a simple operational amplifier (Op-Amp) using Cadence Virtuoso. Participants learned how to:

- Create a schematic of the circuit.
- Simulate the circuit for performance evaluation.
- Transition from schematic to layout and ensure design compliance.

Day 2 – 21.01.2025
Afternoon Session: 02:00 PM to 05:00 PM
Topic: Hands on Session on Analog Circuit

Introduction to Analog Circuits:

- Mr. Navaneethakrishnan explained the foundational concepts of analog circuits, including operational amplifiers, filters, and feedback mechanisms.
- He emphasized the role of analog circuits in modern electronics and their integration with digital systems.

- **Practical Design Techniques:**

- Participants were introduced to practical design methodologies and the significance of component selection in building efficient circuits.
- Common challenges in circuit design were discussed, along with best practices to mitigate these issues.

Hands-on Training with Simulation Tools:

- The session included a demonstration of industry-standard tools for circuit simulation, such as Cadence OrCAD and MATLAB.
- Attendees performed real-time simulations of analog circuits under Mr. Navaneethakrishnan's guidance, gaining hands-on experience in analyzing circuit behavior.

Application-Oriented Approach:

- Real-world applications of analog circuits in areas like signal processing, power management, and communication systems were highlighted.
- Case studies were presented to show how analog circuits are implemented in commercial products.

Q&A and Interaction:

- Mr. Navaneethakrishnan encouraged active participation and addressed queries from students, offering solutions and sharing his industry experience.

Outcomes of the Session:

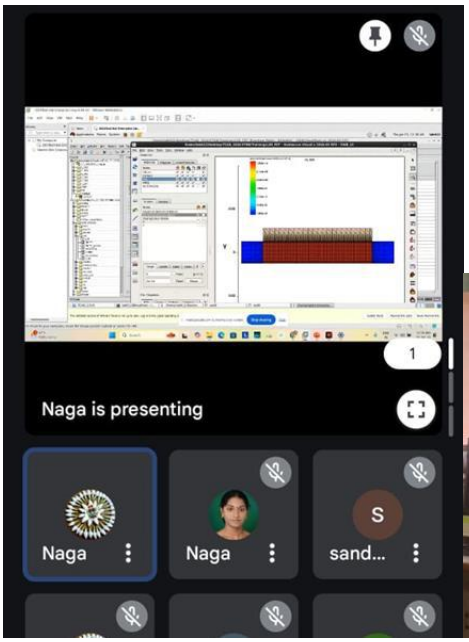
- Participants gained practical exposure to analog circuit design and troubleshooting.
- The session bridged theoretical knowledge with practical applications, enhancing the understanding of circuit analysis and simulation.
- Students developed an appreciation for the importance of analog design in various engineering domains.

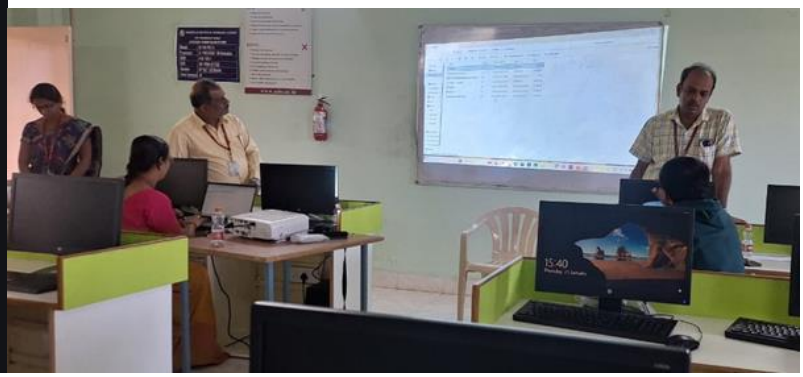
Feedback:
The session was highly appreciated by attendees, who found it both informative and engaging. Participants highlighted the clarity of Mr. Navaneethakrishnan's explanations and his ability to connect theoretical concepts with practical examples.
Conclusion:
The hands-on session conducted by Mr. Navaneethakrishnan proved to be an enriching experience for all attendees. It not only deepened their knowledge of analog circuits but also inspired them to explore further applications in the field of electronics. Such industry-focused initiatives significantly contribute to the professional development of students and faculty members alike.

Felicitation of Resource person:

Day 3 – 22.01.2025
Morning Session : 10:00 AM to 01:00 PM
Resource Person: Dr Narasimhulu Thoti Scientific Researcher Microelectronics Research and University of Oulu 90570 Finland.
Topic : Working with Sentaurus/ Synopsis TCAD Tool for modelling semiconductor devices

Dr. Narasimhulu Thoti, a prominent scientific researcher at the Microelectronics Research Unit, University of Oulu, Finland, is recognized for his expertise in modeling and simulation of semiconductor devices. His research primarily involves the application of the Sentaurus Technology Computer-Aided Design (TCAD) tool developed by Synopsys, an advanced platform for simulating the behavior and properties of semiconductor devices.





Overview of Sentaurus/Synopsys TCAD:
Sentaurus TCAD is a state-of-the-art simulation tool designed to model semiconductor device physics and processes. It integrates physical models to provide insights into the behavior of advanced semiconductor devices under various conditions. The toolset includes modules for:

- Process simulation: Models fabrication steps like ion implantation, diffusion, and annealing.
- Device simulation: Studies electrical, thermal, and optical performance.
- Visualization: Displays 2D/3D device geometries and simulation results.
- Research Focus and Applications

Dr. Thoti's research focuses on utilizing Sentaurus TCAD to address challenges in microelectronics and develop innovative semiconductor solutions. His key areas of interest include:

Device Optimization and Scaling: Dr. Thoti employs Sentaurus to explore the effects of scaling down semiconductor devices to nanoscale dimensions. His research aims to optimize transistor performance by studying parameters such as short-channel effects, leakage currents, and device reliability.

- **Advanced Material Integration:** The integration of novel materials like silicon-germanium (SiGe), gallium nitride (GaN), and two-dimensional materials such as graphene is a significant part of Dr. Thoti's work. Sentaurus helps simulate their behavior in devices, ensuring compatibility and performance enhancements.
- **Energy-Efficient Devices:** With the increasing demand for energy-efficient electronics, Dr. Thoti's work emphasizes low-power device design. Using Sentaurus, he evaluates designs for their energy consumption, thermal stability, and overall performance.
- **Process Variability Analysis:** Variations during fabrication processes can impact device performance. Dr. Thoti uses TCAD simulations to analyze these variations, ensuring robust device design and reduced manufacturing defects.
- **Significance of the Research:** The use of TCAD tools like Sentaurus bridges the gap between theoretical device concepts and practical implementation.

Dr. Thoti's work contributes to:

- Accelerating the design cycle by reducing the need for extensive experimental prototyping.
- Providing a deeper understanding of device physics through simulation.
- Enhancing the performance and reliability of next-generation semiconductor devices

Day 3 – 22.01.2025
Afternoon Session : 02:00 PM to 05:00 PM
Resource Person: Dr. Narasimhulu Thoti Scientific Researcher Microelectronics Research and University of Oulu 90570 Finland.

Topic : Device Design Examples through Sentaurus TCAD

Device Design Examples through Sentaurus TCAD. Dr. Thoti's research highlights the application of Sentaurus TCAD in the following key areas:

1. MOSFET Design and Optimization:
Objective: To improve the performance of Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) by exploring alternative materials and geometries.
Example Work: Dr. Thoti has designed MOSFETs with high-k gate dielectrics, low-resistance source/drain contacts, and advanced channel architectures like FinFETs and nanowire FETs. Sentaurus TCAD simulations allowed precise analysis of subthreshold slope, drain-induced barrier lowering (DIBL), and mobility enhancement.

2. Power Semiconductor Devices:
Objective: Develop power devices, such as IGBTs (Insulated Gate Bipolar Transistors) and SiC MOSFETs, to achieve higher efficiency in power electronics.
Example Work: Sentaurus TCAD was employed to simulate electric field distribution, thermal performance, and breakdown voltage in silicon carbide (SiC) and gallium nitride (GaN)-based power devices. His results demonstrate significant improvements in power density and reliability.

3. Solar Cells:
Objective: Enhance the efficiency of photovoltaic devices through material and structural innovation.
Example Work: Dr. Thoti used Sentaurus TCAD to design thin-film solar cells with improved light absorption and carrier collection. Simulations focused on tandem solar cells and novel perovskite materials, achieving record efficiency predictions under specific conditions.

4. MEMS Devices:
Objective: Integrate Micro-Electro-Mechanical Systems (MEMS) with advanced semiconductors for applications like sensors and actuators.
Example Work: His research simulated piezoresistive MEMS sensors using Sentaurus TCAD, optimizing sensitivity, mechanical stability, and energy consumption for IoT applications.

Day 4 – 23.01.2025
Morning Session: 10:00 AM to 01:00 PM
Resource Person: Dr. Narasimhulu Thoti, Scientific Researcher Microelectronics Research and University of Oulu 90570 Finland.
Topic: Physical Modeling of Device through Sentaurus TCAD & Characterization of Semiconductor devices using Sentaurus TCAD

Research Focus: Physical Modeling and Characterization Using Sentaurus TCAD

1. Overview of Sentaurus TCAD:

Sentaurus TCAD (Technology Computer-Aided Design) is a powerful simulation framework used for the design and analysis of semiconductor devices. It enables researchers to perform physical modeling, simulate device behavior, and characterize performance before actual fabrication, thereby reducing development costs and time.

Key features of Sentaurus TCAD include:

- Support for multidimensional simulations (1D, 2D, and 3D).
- Advanced physical models for charge transport, heat dissipation, and quantum effects.
- Capabilities to simulate novel materials and devices, such as compound semiconductors, heterostructures, and nanoscale devices.

2. Physical Modeling of Semiconductor Devices:

Dr. Thoti's research leverages Sentaurus TCAD to develop highly accurate physical models of various semiconductor devices. The key steps in this process include:

- **Device Structure Design:** Using advanced geometry editors and mesh generators in Sentaurus, Dr. Thoti constructs detailed 2D and 3D device structures.
- **Material Parameterization:** Incorporating material properties, such as bandgap, mobility, and recombination coefficients, for materials like Si, Ge, GaN, and other III-V compounds.
- **Transport Mechanism Modeling:** Simulating carrier dynamics (drift-diffusion, hydrodynamic transport, and quantum tunneling) and studying the effects of these mechanisms on device performance.
- **Process Simulations:** Employing process simulation tools within Sentaurus TCAD to model ion implantation, diffusion, oxidation, and other fabrication steps.

3. Characterization of Semiconductor Devices:

Using Sentaurus TCAD, Dr. Thoti performs comprehensive characterization of semiconductor devices, including:

- **Electrical Characterization:** Simulating current-voltage (I-V) characteristics, capacitance-voltage (C-V) profiles, and threshold voltage shifts to assess device behaviour under various biasing conditions.
- **Thermal Analysis:** Modeling self-heating effects and heat dissipation to evaluate device reliability under high-power operation.
- **Optical Analysis:** Investigating photonic interactions in optoelectronic devices, such as solar cells and photodetectors.
- **Reliability Testing:** Analysing degradation mechanisms, including hot carrier injection (HCI), bias temperature instability (BTI), and time-dependent dielectric breakdown (TDDB).

Day 4 – 23.01.2025

Afternoon Session: 02:00 PM to 05:00 PM
Resource Person: Dr Narasimhulu Thoti Scientific Researcher Microelectronics Research and University of Oulu 90570 Finland.
Topic : Physical Design Flow

Physical Design Flow refers to the transformation of a circuit's logical representation into its physical layout, which can then be fabricated on a silicon wafer. This process is integral to the development of modern integrated circuits (ICs) and involves various stages, including:

- **Partitioning and Floorplanning:** Breaking down the design into smaller blocks and arranging them within a defined chip area while optimizing for performance, power, and area.
- **Placement:** Assigning precise locations to each cell or module in the design, ensuring minimum delay and power consumption.
- **Clock Tree Synthesis (CTS):** Designing a clock distribution network to ensure synchronized operation across the chip.
- **Routing:** Establishing connections between components using metal layers, adhering to design rules to minimize resistance, capacitance, and interference.
- **Design Rule Checking (DRC):** Verifying that the layout adheres to the fabrication process's geometric and electrical constraints.
- **Timing Analysis:** Ensuring the design meets timing constraints to avoid delays or functional errors.

Felicitation of Resource Person:

Day 5 : 24.01.2025

Morning Session: 10:00 AM to 01:00 PM
Resource Person: Dr. V. Bharath Sreenivasulu, Assistant Professor, Department of Electronics & Communication Engineering, Manipal University.

Topic : VLSI Emerging Devices like FinFET nanowire, nanosheet for CMOS Applications

As CMOS technology progresses towards nano-dimensions, conventional planar transistors are facing significant challenges due to short-channel effects, leakage currents, and limitations in scaling. The demand for energy-efficient, high-performance, and highly scalable devices has driven innovations in VLSI (Very-Large-Scale Integration) technology. Emerging transistor architectures like FinFETs, nanowires, and nanosheets are becoming the frontrunners in overcoming these limitations and enabling the next generation of CMOS applications.

Emerging Devices in VLSI:

1. **FinFET (Fin Field Effect Transistor)**

FinFETs are one of the most widely adopted solutions to the scaling limitations of planar MOSFETs. They feature a three-dimensional structure with a "fin"-like channel that rises above the substrate.

Key Characteristics:

- Enhanced electrostatic control of the gate over the channel.
- Reduction in leakage current due to better gate control.
- High drive current and switching speeds.

Applications:

FinFETs are extensively used in modern processors and memory technologies due to their energy efficiency and scalability to sub-10nm nodes.

2. Nanowire Transistors

Nanowires take transistor scaling a step further by utilizing cylindrical or rectangular channel structures that offer better gate control compared to FinFETs.

Advantages:

- Full gate-surrounding architecture for superior electrostatic control.
- High on/off current ratios.
- Improved performance for ultra-scaled dimensions.

Applications:

Nanowires are suitable for low-power, high-density CMOS applications, making them a potential candidate for future system-on-chip (SoC) technologies.

3. Nanosheet Transistors:

Nanosheets are an evolution of nanowire transistors and are designed to address the limitations in current flow associated with nanowires. These devices stack flat, wide sheets as channels, offering enhanced drive currents while retaining excellent electrostatic control.

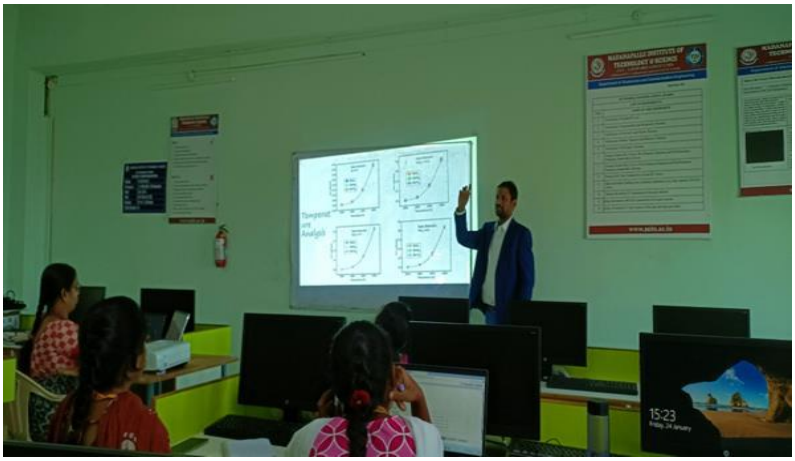
Key Features:

- Improved drive current compared to nanowires.
- Compatibility with advanced manufacturing techniques like extreme ultraviolet (EUV) lithography.

Applications:

- Nanosheets are considered the next step in CMOS transistor scaling and are expected to dominate technology nodes below 3nm.
- Advantages of Emerging VLSI Devices for CMOS Applications
- **Better Short-Channel Control:** Devices like FinFETs, nanowires, and nanosheets mitigate short-channel effects, allowing further scaling of transistors.
- **Energy Efficiency:** These structures reduce leakage currents and enhance energy efficiency, crucial for battery-operated and IoT devices.
- **Scalability:** Their three-dimensional designs offer greater scalability, making them viable for sub-10nm nodes and beyond.
- **Challenges and Future Directions:** While these emerging devices address many issues associated with traditional CMOS technology, challenges remain
- **Fabrication Complexity:** Advanced manufacturing techniques such as EUV lithography are required, increasing production costs.
- **Material Limitations:** The integration of novel materials like high-k dielectrics and low-resistance contacts is crucial for further performance improvements.

- **Reliability Concerns:** As device dimensions shrink, maintaining reliability and minimizing variability become critical concerns.



Day 5 – 24.01.2025

Afternoon Session – 02:00 PM to 05:00 PM

Resource Person: Dr. V. Bharath Sreenivasulu, Assistant Professor, Department of Electronic & Communication Engineering, Manipal University

Topic : Hands on with Nanohub tool for 2D material based FETS

Nanohub is an online platform providing a comprehensive suite of simulation tools and resources for research and education in nanotechnology. It allows users to access various simulation models for different nanomaterials and devices, offering capabilities in modeling, characterization, and performance evaluation. It has become an essential tool for researchers and educators working with nanoscale materials and devices, providing a seamless environment for simulation without the need for extensive hardware setups.

Session Highlights:

Introduction to 2D Materials and FETs

Dr. Sreenivasulu began by introducing the concept of 2D materials, which are materials that consist of a single or few layers of atoms. Their remarkable electronic properties, such as high carrier mobility, flexibility, and strong quantum confinement, make them ideal candidates for the development of future FETs. He explained the advantages of using 2D materials over conventional silicon, highlighting the potential for faster, more efficient, and miniaturized devices.

The Role of Nanohub in FET Design

The session focused on the use of Nanohub tools for simulating and analyzing 2D material-based FETs. Dr. Sreenivasulu demonstrated how to access and use the tools on Nanohub, showing the basic steps to set up simulations for 2D FETs. He explained the importance of simulating material properties such as band structure, charge transport, and device behavior under different operating conditions. Participants were introduced to specific tools such as Quantum ATK, NanoTCAD, and Sentaurus for detailed device simulations.

Hands-on Session:

Dr. Sreenivasulu guided the participants through a series of practical exercises using Nanohub's tools. They began by selecting appropriate 2D materials, such as MoS2 or graphene, and inputting parameters like material thickness, gate dielectric properties, and bias conditions. The participants then conducted simulations to analyze key characteristics such as the subthreshold slope, on-off current ratio, and threshold voltage of the FETs. These simulations helped the participants understand the impact of material selection and device design on the overall performance of the FET.

Challenges in 2D Material-Based FETs:

During the session, Dr. Sreenivasulu discussed some of the challenges associated with 2D material-based FETs, such as issues with contact resistance, scalability, and material stability. He emphasized the need for advanced simulation techniques to predict and mitigate these issues before moving to experimental fabrication. The role of Nanohub tools in optimizing device design and identifying potential failure points before physical testing was also highlighted.

Future Prospects and Applications:

Dr. Sreenivasulu concluded the session by discussing the future applications of 2D material-based FETs, such as in flexible electronics, low-power devices, and high-performance computing. He stressed that understanding the intricacies of 2D material-based device behavior through simulations is crucial for accelerating the development of these novel technologies.

Felicitation of Resource Person:

Newspaper Clips:

ఈనాడు
epaper.eenadu.net

ఆధునిక సాంకేతికతపై అవగాహన

అంగళ్లు (కురబలకోట), న్యూస్‌టుడే : ఆధునిక సాంకేతికతపై అవగాహన పెంచుకోవాలని బెంగళూరుకు చెందిన సీనియర్ ఆప్లికేషన్ ఇంజినీర్ నవనీతకృష్ణన్ తెలిపారు. మిట్స్ కళాశాల ఆవరణలో కార్యశాలను సోమవారం వైస్ ప్రిన్సిపల్ డాక్టర్ రామనాథన్ ప్రారంభించారు. కార్యక్రమంలో విభాగాధిపతి డాక్టర్ రాజశేఖరన్, కోఆర్డినేటర్ డాక్టర్ నాగజ్యోతి, డాక్టర్ నాగశ్వేత, చరణ్ తదితరులు పాల్గొన్నారు.

Date : 21/01/2025 EditionName :
ANDHRA PRADESH(ANNAMAYYA)
PageNo :

నూతన ఆలోచనలతో ముందుకు సాగాలి

సమావేశంలో మాట్లాడుతున్న రిసోర్సుపర్సన్ నవనీత్ కృష్ణన్

కురబలకోట, జనవరి 20(ఆంధ్రజ్యోతి): విద్యార్థులు, అధ్యాపకులు నూతన ఆలోచనలతో ముందుకు సాగాలని రిసోర్సుపర్సన్ నవనీత్ కృష్ణన్ పేర్కొన్నారు. సోమవారం మండలంలోని మిట్స్ ఇంజనీరింగ్ కళాశాలలో సెమికండక్టర్ తయారీకి ఉపయోగపడే సాధనాల ఆచరణాత్మక ఉపయోగంపై వర్క్‌షాప్ నిర్వహించారు. ఈ సందర్భంగా ఆయన మాట్లాడుతూ పరిశ్రమలు అవసర మిశ్రమాన్ని దూరం తగ్గించడానికి పరిశోధనలు చేపట్టి మంచి ఫలితాలను సాధించాలని కోరారు. ప్రస్తుతం సాఫ్ట్‌వేర్ రంగంతో పోల్చితే ఈసీఈ రంగంలో మెరుగైన ఉద్యోగ అవకాశాలు ఉన్నాయన్నారు. ప్రధాని మోదీ స్వాబ్ సిదీని మంజూరు చేశారని, దీనిలో ఎంబెడెడ్ వీఎల్‌ఎస్‌ఐడీఏ టెక్నాలజీలు ఎంతగానో దోహద పడుతాయని వాటిపై పట్టు సాధించాలని సూచించారు. ఈ కార్యక్రమంలో విభాగాధిపతి రాజశేఖరన్, నాగజ్యోతి, నాగశ్వేత, చరన్ తదితరులు పాల్గొన్నారు.

మిట్స్ కళాశాలలో సెమీ కండక్టర్ తయారీకి ఈడిపి..
సాధనాల ఆచరణాత్మక ఉపయోగం అను అంశంపై..
ఐదు రోజుల వర్క్ షాప్ ప్రారంభం..

ముఖ్యఅతిథిగా హాజరైన నవనీత కృష్ణన్..

వైస్ ప్రిన్సిపాల్ డాక్టర్ రామనాథన్ వెల్లడి..

మదనపల్లి **(నిమా సూర్య)**

మదనపల్లె ఇన్‌స్టిట్యూట్ ఆఫ్ టెక్నాలజీ, సైన్స్ (మిట్స్) కళాశాల నందు సెమీకండక్టర్ తయారీకి ఈడిపి సాధనాల ఆచరణాత్మక ఉపయోగం అను అంశం పై ఐదు రోజుల వర్క్‌షాప్ ను సోమవారం ప్రారంభించారు. వర్క్‌షాప్ ను ప్రతిష్టాత్మకమైన ఐఈఈఈ వారు అధ్వర్యంలో నిర్వహించినట్లు కళాశాల వైస్ ప్రిన్సిపాల్ డాక్టర్ రామనాథన్ అన్నారు. ఈ కార్యక్రమానికి ముఖ్య అతిథిగా నవనీతకృష్ణన్, సీనియర్ అప్లికేషన్ ఇంజనీర్, డిజైన్ ఈ డి ఏ సపోర్ట్, ఎంటువుల్ టెక్నాలజీస్ - బెంగుళూరు పాల్గొన్నారు. కార్యక్రమంలో ఆయన మాట్లాడుతూ పరిశ్రమలకు,అకడమిక్స్ కి మధ్య అంతరంను తగించడానికి, పరిశ్రమల సమస్యల పై రీసెర్చ్ ద్వార పరిష్కరించి సరైన ఆలోచనలతో ముందుకెళ్ళి, మంచి ఫలితాలను రాబట్టడా ఇటువంటి టూల్స్ ఎంతగానో ధోహద పడతాయని తెలిపారు. ఇటువంటి అడ్వాన్స్ డ్ టూల్స్ కొనుగోలు చే పీజీ స్టూడెంట్స్ పరిశోధనలు అతిత్వరగా పూర్తి చేయుటకు మంచి అవకాశం ఉందన్నారు. ప్రస్తుత పోటీప్రపంచంలో సాఫ్ట్‌వేర్ ఉద్యోగాలతో పోలిస్తే ఈసీఈ విభాగము విద్యార్థులకు మెరుగైన అవకాశాలు ఉన్నాయని, ముఖ్యంగా వి.ఎల్.ఎస్.ఐ, ఎంబెడెడ్ సిస్టమ్స్ పై మెందుగా ఉన్నాయన్నారు. ప్రస్తుత మన ప్రధానమంత్రి నరేంద్ర మోదీ ఫ్యాబ్ సిటీస్ మంజూరు చేశారని,అవన్ని నిర్మాణ దశలో ఉన్నాయని త్వరలో అవి అందుబాటులోకి వస్తాయన్నారు.(వి.ఎల్.ఎస్.ఐ ఈడిఏ) టూల్స్ పై మనం అవగాహన పెంచుకొని,పరిశోధనలు చేయాలనీ ఆయన అన్నారు. ప్రస్తుతం ఏ ఫ్యాబ్రికేషన్‌కి అయినా మనం (ఇంటెల్) కంపేనీపై ఆధారపడి ఉన్నామన్నారు. మన ఇండియాలో కొత్త టెక్నాలజీకి సరైన అవగాహన లేదని ఇటు వంటి వర్క్‌షాప్‌లకు హాజరవడం వళ్ల ఇండస్ట్రీలో జరుగుతున్న పరిశోధనలనుతొ విద్యార్థులు తెలుసుకొని తద్వారా అధునాతన సాధనాలతో నూతన పరిశోధనలు చేయాలన్నారు. ఈ కార్యక్రమంలో విభాగాధిపతి డాక్టర్ రాజశేఖరన్, కో ఆర్డినేటర్ డాక్టర్ నాగ జ్యోతి, డాక్టర్ నాగశ్వేత, చరన్ తదితరులు పాల్గొన్నారు.

ఐ.ఈ.ఈ.ఈ ఆధ్వర్యంలో
మిట్స్‌లో వర్క్‌షాప్ ప్రారంభం

కురబలకోట, జనవరి 21(నేటి మానవేతర ప్రతినిధి): మదనపల్లె ఇన్‌స్టిట్యూట్ ఆఫ్ టెక్నాలజీ అండ్ సైన్స్ (మిట్స్ కళాశాల) నందు సెమీకండక్టర్ తయారీకి (ఈడిపి) సాధనాల ఆచరణాత్మక ఉపయోగం అనే అంశంపై ఐదురోజుల వర్క్‌షాప్‌ను సోమవారం ప్రారంభించారు. వర్క్‌షాప్‌ను ప్రతిష్టాత్మకమైన (ఐతఈతఈ) వారు అధ్వర్యంలో నిర్వహించినట్లు కళాశాల వైస్ ప్రిన్సిపాల్ డాక్టర్ రామనాథన్ అన్నారు. ఈ కార్యక్రమానికి ముఖ్య అతిథిగా నవనీత కృష్ణన్, సీనియర్ అప్లికేషన్ ఇంజనీర్,డిజైన్ మరియు ఈడీఏ సపోర్ట్,ఎంటువుల్ టెక్నాలజీస్-బెంగుళూరు పాల్గొన్నారు. ఈ కార్యక్రమంలో ఆయన మాట్లాడుతూ పరిశ్రమలకు, అకడమిక్స్‌కి మధ్యంతరాన్ని తగించడానికి, పరిశ్రమల సమస్యలపై రీసెర్చ్ ద్వార పరిష్కరించి సరైన ఆలోచనలతో ముందుకెళ్ళి,మంచి ఫలితాలను రాబట్టడానికి ఇటువంటి టూల్స్ ఎంతగానో ధోహదపడతాయని పేర్కొన్నారు. ఇటువంటి అడ్వాన్స్ డ్ టూల్స్ కొనుగోలు చేసి పీజీ స్టూడెంట్స్ పరిశోధనలు అతిత్వరగా పూర్తి చేయుటకు మంచి అవకాశం ఉందన్నారు.ప్రస్తుత పోటీ ప్రపంచంలో సాఫ్ట్‌వేర్ ఉద్యోగాలతో పోలిస్తే ఈసీఈ విభాగము విద్యార్థులకు మెరుగైన అవకాశాలు ఉన్నాయని,ముఖ్యంగా వి.ఎల్.ఎస్.ఐ, ఎంబెడెడ్ సిస్టమ్స్‌పై మెందుగా ఉన్నాయన్నారు.ప్రస్తుత మన ప్రధానమంత్రి నరేంద్ర మోదీ ఫ్యాబ్ సిటీస్ మంజూరు చేశారని, అవన్ని నిర్మాణ దశలో ఉన్నాయని త్వరలో అవి అందుబాటులోకి వస్తాయన్నారు.(వి.ఎల్.ఎస్.ఐ ఈడిఏ) టూల్స్‌పై మనం అవగాహన పెంచుకొని, పరిశోధనలు చేయాలనీ అయన అన్నారు. ప్రస్తుతం ఏ ఫ్యాబ్రికేషన్‌కి అయినా మనం (ఇంటెల్) కంపేనీపై ఆధారపడి ఉన్నామన్నారు. మన ఇండియాలో కొత్త టెక్నాలజీకి సరైన అవగాహన లేదని ఇటు వంటి వర్క్‌షాప్‌లకు హాజరవడం వళ్ల ఇండస్ట్రీలో జరుగుతున్న పరిశోధనలను విద్యార్థులు తెలుసుకొని తద్వారా అధునాతన సాధనాలతో నూతన పరిశోధనలు చేయాలన్నారు.ఈ కార్యక్రమంలో విభాగాధిపతి డాక్టర్ రాజశేఖరన్,కో-ఆర్డినేటర్ డాక్టర్ నాగజ్యోతి,డాక్టర్ నాగశ్వేత, చరన్ తదితరులు పాల్గొన్నారు.

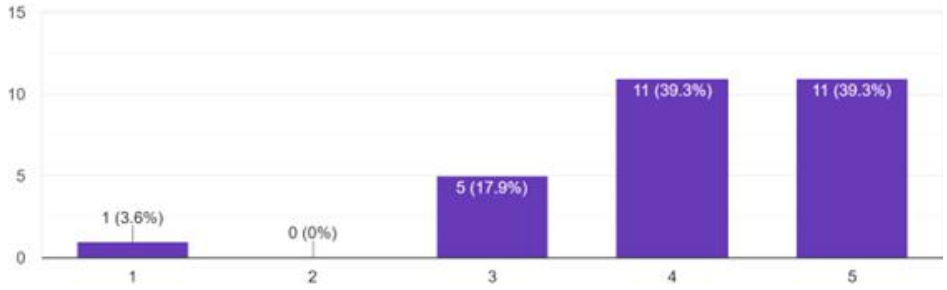
ఐఈఈఈ ఆధ్వర్యంలో మిట్స్ కళాశాల వర్క్‌షాప్ ప్రారంభం

మదనపల్లె,జనవరి 20(కురుక్షేత్రం ప్రతినిధి) :అంగళ్లు సమీపంలోని మదనపల్లె ఇన్‌స్టిట్యూట్ ఆఫ్ టెక్నాలజీ అండ్ సైన్స్ (మిట్స్ కళాశాల) నందు సెమీకండక్టర్ తయారీకి (ఈడిపి) సాధనాల ఆచరణాత్మక ఉపయోగం అనే అంశంపై ఐదురోజుల వర్క్‌షాప్ ను సోమవారం ప్రారంభించారు.వర్క్‌షాప్ ను ప్రతిష్టాత్మకమైన (ఐతఈతఈ) వారు అధ్వర్యంలో నిర్వహించినట్లు కళాశాల వైస్ ప్రిన్సిపాల్ డాక్టర్ రామనాథన్ అన్నారు. ఈ కార్యక్రమానికి ముఖ్య అతిథిగా నవనీత కృష్ణన్, సీనియర్ అప్లికేషన్ ఇంజనీర్,డిజైన్ మరియు ఈడీఏ సపోర్ట్, ఎంటువుల్ టెక్నాలజీస్ - బెంగుళూరు పాల్గొన్నారు. ఈ కార్యక్రమంలో ఆయన మాట్లాడుతూ పరిశ్రమలకు మరియు అకడమిక్స్‌కి మధ్యంతరాన్ని తగించడానికి మరియు పరిశ్రమల సమస్యలపై రీసెర్చ్ ద్వార పరిష్కరించి సరైన ఆలోచనలతో ముందుకెళ్ళి,మంచి ఫలితాలను రాబట్టడానికి ఇటువంటి టూల్స్ ఎంతగానో ధోహదపడతాయని పేర్కొన్నారు. ఇటువంటి అడ్వాన్స్ డ్ టూల్స్ కొనుగోలు చేసి పీజీ స్టూడెంట్స్ పరిశోధనలు అతిత్వరగా పూర్తి చేయుటకు మంచి అవకాశం ఉందన్నారు.ప్రస్తుత పోటీ ప్రపంచంలో సాఫ్ట్‌వేర్ ఉద్యోగాలతో పోలిస్తే ఈసీఈ విభాగము విద్యార్థులకు మెరుగైన అవకాశాలు ఉన్నాయని,ముఖ్యంగా వి.ఎల్.ఎస్.ఐ మరియు ఎంబెడెడ్ సిస్టమ్స్ పై మెందుగా ఉన్నాయన్నారు.ప్రస్తుతం మన ప్రధానమంత్రి నరేంద్ర మోదీ ఫ్యాబ్ సిటీస్ మంజూరు చేశారని,అవన్ని నిర్మాణ దశలో ఉన్నాయని త్వరలో అవి అందుబాటులోకి వస్తాయన్నారు.(వి.ఎల్.ఎస్.ఐ ఈడిఏ) టూల్స్ పై మనం అవగాహన పెంచుకొని,పరిశోధనలు చేయాలనీ అయన అన్నారు. ప్రస్తుతం ఏ ఫ్యాబ్రికేషన్‌కి అయినా మనం (ఇంటెల్) కంపేనీపై ఆధారపడి ఉన్నామన్నారు. మన ఇండియాలో కొత్త టెక్నాలజీకి సరైన అవగాహన లేదని ఇటు వంటి వర్క్‌షాప్‌లకు హాజరవడం వళ్ల ఇండస్ట్రీలో జరుగుతున్న పరిశోధనలను విద్యార్థులు తెలుసుకొని తద్వారా అధునాతన సాధనాలతో నూతన పరిశోధనలు చేయాలన్నారు. ఈ కార్యక్రమంలో విభాగాధిపతి డాక్టర్ రాజశేఖరన్,కో-ఆర్డినేటర్ డాక్టర్ నాగజ్యోతి,డాక్టర్ నాగశ్వేత,చరన్ తదితరులు పాల్గొన్నారు.

Feedback from Students:

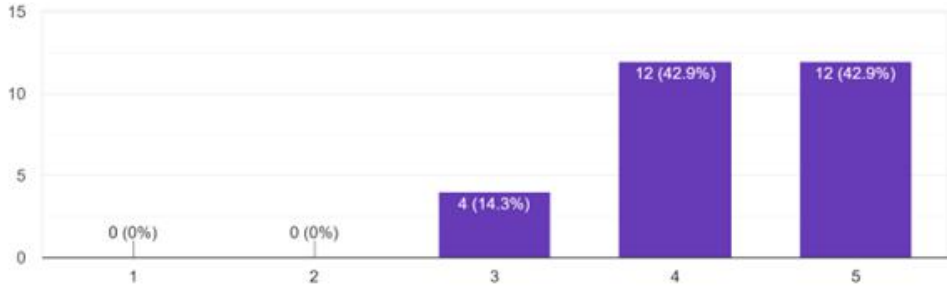
1. The interactive session was scheduled at a suitable time

28 responses



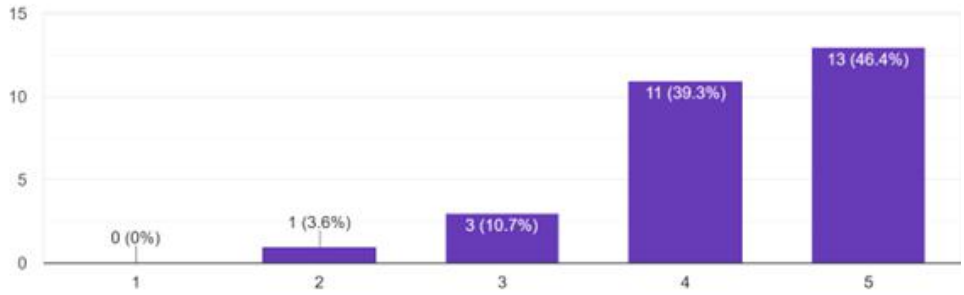
2. The interaction was useful and resource person explanation.

28 responses



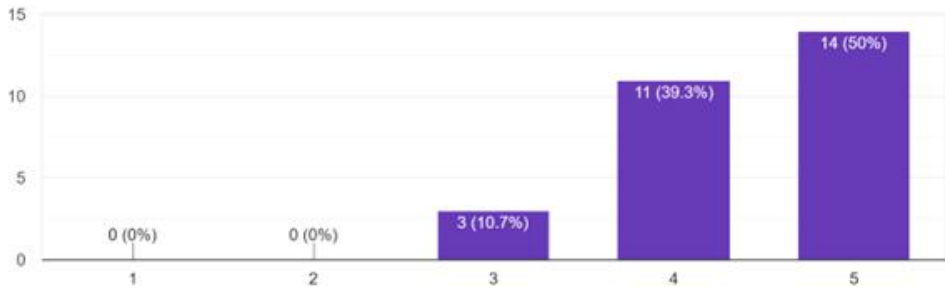
3. The information in the interaction was presented in a clear and organized manner.

28 responses



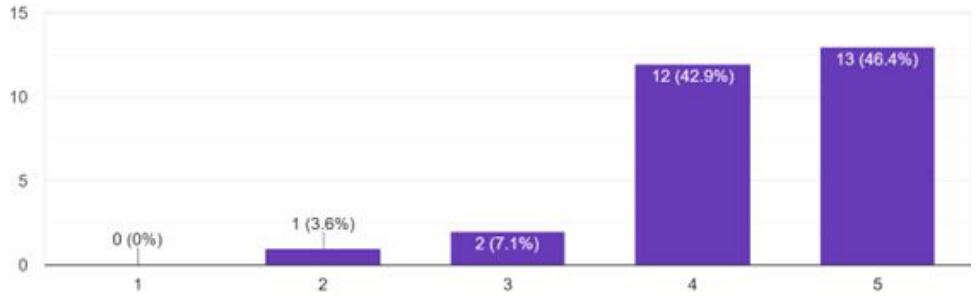
4. The presenter responded to questions an informative, appropriate and satisfactory manner.

28 responses



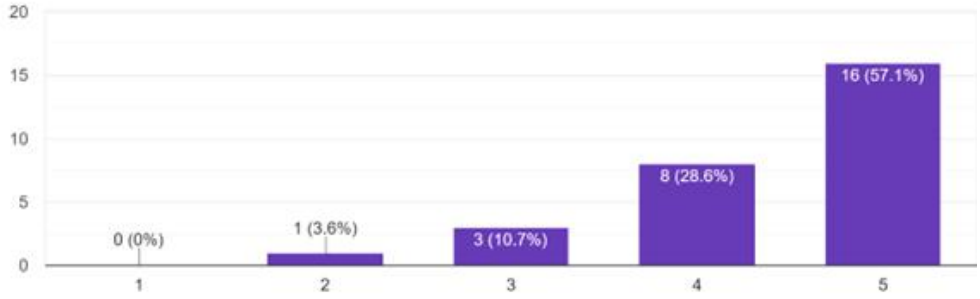
5. your impression of facilities provided by the institute for interaction.

28 responses



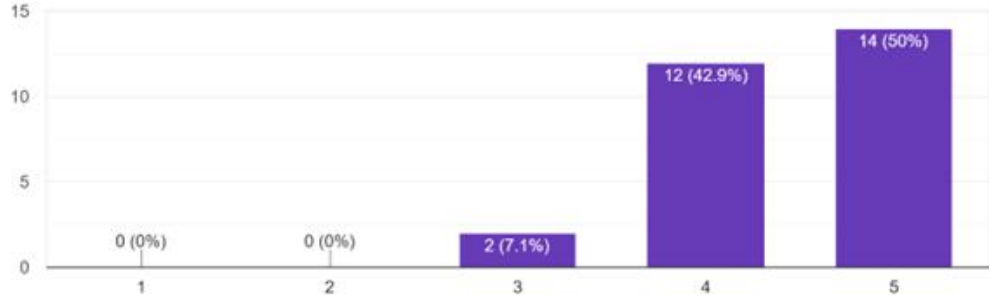
6. Overall, the session was informative and valuable.

28 responses



7. In what ways could this interaction have been improved to better suit your needs?

28 responses



8. Any Other Comments

21 responses