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## Circular Dated: 31-01-2019

All the students III- B.Tech-ECE are here by informed that "Challenges in Signal and Power Integrity for Server Designs" is going to be conducted on 02-02-2019 with the concept of learning Challenges in Signal Integrity for Server Design.

PRINCIPAL University of Filling States Politic Rock, Resh Boo J, Angalu MADANAPALLE-617 325, AP

Copy to: 1. All the III- B.Tech-ECE Class rooms.

2. Circular to Notice Board

#### MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE (UGC - AUTONOMOUS)



Submitted by: Dr. Ranjeet Kumar, Senior Assistant Professor, Electronics and Communication Engineering

Resource person: Dr. Nikita Ambasana, Team Lead (Intel Corporation), Bangalore Submitted by: Dr. Ranjeet Kumar and Dr.
Ranjan Kumar Mahapatra
Participants: 3rd Year ECE B.Tech students
& Faculty No. of Students participated-132
The Department of Electronics and Communication Engineering initiated a one-day Seminar on "Challenges in Signal and Power Integrity for Server Designs" for the students of MITS on 02-02-2019.

Dr. Ranjeet Kumar, Senior Assistant Professor, ECE welcomed all the dignitaries, resource person, faculty members, students and expressed his gratitude towards Management and Principal for giving permission to organize the seminar. Vice Principal - Academics Dr. P. Ramanathan talked about the benefits of this seminar. Later, Dean Dr K.R. Kashwan emphasized on learning technologies and correlating them in different applications.

The seminar was delivered Session 1: Challenges in Signal Integrity for Server Designs. Session 2: Challenges in Power Integrity Forever. Designs Emphasis was given in the following topics:

- 1. Server.
- 2. Processor.
- 3. Server Design.
- 4. Integrity of signal and power.
- 5. Determining the design parameters.
- 6. High performance.
- 7. Risk assessment.

**Press Clips:** 



### Challenges in Signal and Power Integrity for Server Designs

Madanapalle Institute of Technology and Science conducted a session on Challenges in Signal and Power Integrity for Server Designs for 3rd Year ECE B.Tech students. Resource person was Dr. Nikita Ambasana, Team Lead (Intel Corporation), Bangalore delivered lectures on delivered on Challenges in Signal Integrity for Server Designs and Challenges in Power Integrity Forever. Vice Principal - Academics Dr. P. Ramanathan talked about the benefits of this seminar. Later, Dean Dr K.R. Kashwan emphasized on learning technologies and correlating them in different applications. Principal dr. C. Yuvaraj and the HOD of the department attended the program.

PRINCIP chaology & Science ut l'alla, Kashi Road, Angellu 100/0119/01E-517 325, A.P



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# MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

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(Affiliated to JNTUA, Ananthapuramu& Approved by AICTE, New Delhi) P.B. No:14, Angallu (Village), MADANAPALLE - 517 325. (A.P)

Website: www.mits.ac.in

Department of Electronics and Communication Engineering

### Subject: Seminar on "Challenges in Signal and Power Integrity for Server Designs" Resource Person : Dr. Nikita Ambasana, Team Lead (Intel Corporation), Bangalore

Date: 02-02-2019, 11:00 AM onwards

Venue: Seminar Hall						
	LIST OF ATTENDEES					
S. No	Name	Designation/Roll No	. Signature			
1	ADITHYA PRASAD REDDY. B	16691A0402	A			
2	AFREEN KHANAM. P	16691A0403	Atl			
3	AKHILA. M	16691A0404	N			
4	AMULYA JACINTHA. K	16691A0405	Au			
5	ANIL KUMAR. P	16691A0406	And Kun			
6	ANJALI. T	16691A0407	And			
7	ARAVIND SWAMY. C	16691A0408	Arravin2			
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9	ARUN KUMAR REDDY. K	16691A0411	ADV			
10	ASHOK CHAKRAVARTHI. V	16691A0412	subob.			
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